TAM-104

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: T. TANIMOTO, et al

Serial No.: Not Yet Assigned

Filed: On Even Date

For: SYSTEM DEVELOPMENT METHOD AND DATA PROCESSING SYSTEM

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

April 28, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In the matter of the above-identified application, applicants are submitting herewith copies of any foreign or publication (i.e. articles) documents. Applicants also submit that copies of any U.S. Patents are not being submitted since these documents can be easily obtained by the United States Patent and Trademark Office as listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted with the new application.

Although some of the documents listed on the attached form equivalent to Form PTO-1449 are not in the English language, the requirement of 37 CFR 1.98 (a)(3) for a concise explanation of the relevance is satisfied by the attached English language abstracts and/or the discussion of these documents in the specification, for example on page 1.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Mattingly, Stanger, Malur & Brundidge, P.C. Deposit Account No. 50-1417 (Case: TAM-104), and please credit any excess fees to such deposit account.

Respectfully submitted,

Mattingly, Stanger & Malur, Brundidge, P.C.

John R. Mattingly
Registration No. 30,293

JRM/nac

Attachments

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. TAM-104	SERIAL NO. 10/533062
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT T. TANIMOTO, et al	
		FILING DATE April 28, 2005	GROUP

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Abstract	
							Yes	No
	AG	2002-279333	9/2002	JP			X	
	AH	2000-035898	2/2000	JP			X	
	AI	07-084832	03/1995	JP			X	
	AJ	2 317 245 A	3/1998	GB			X	
	AK	10-116302	6/1998	JP			X	
	AL							
	AM							
	AN							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AO	M. IENAGA, et al.," Seiyo Shori Hardware no Koi Gosei no Tame no Kosoku na Menseki/Jikan Saitekika Algorithm", DA Symposium 2000, Information Processing Society of Japan, 17 July, 2000 (17/07/00), Vol. 2000, No. 8, pages 27 to 32.
	AP	A. NAKATA, et al., "Deriving Parameter Conditions for Periodic Timed Automata Satisfying Real-Time Temporal Logic Formulas", Proc. of IFIP TCP/WG6. 1 Int. Conf. on Formal Techniques for Networked and Distributed Systems (FORTE2001),Kluwer Academic Publishers, 2001.08, pages 151-166.
	AQ	K. WAKABAYASHI, et al., Densoyo LSI o Dosa Gosei de Kaihatsu, Kino Sekkei no Kikan ga 1/10 ni Tanshuku", Nikkei Electronics, Nikkei Business Publications, Inc., 12 February, 1996, No. 655, pages 147-169.
	AR	H. OKEWATARI, et al., "Multi Processor ni yoru Bunsan Shori o Ishiki Shita Senyo Processor Sekkei Shien System SYARDS no Kochiiku", Information Processing Society of Japan Kenkyu Hokoku, Information Processing Society of Japan, 20 January, 1995, Vol. 95, No. 6 (DA-73), pages 105 – 112.
	AS	S. KITAGUCHI, et al., "Jitsujikan Seiyaku o Yusuru Tan'itsu Bus System no JAVA ni yoru Model-ka oyobi Parametric Model Checking o Mochita Sekkei Shuho no Teian", Information Processing Society of Japan Kenkyu Hokoku, Information Processing Society of Japan, 28 Nov. 2002, Vol. 2002, No. 113 (SLDM-107), pages 19 to 24.
	AT	"TAXYS: A Tool For the Development and Verification of Real-Time Embedded Systems" by E. CLOSSE, et al.
	AU	"Design and Implementation of Priority Queuing Mechanism On FPGA Using Concurrent Periodic EFSMs And Parametric Model Checking" by T. KITANI, et al.
	AV	"A Flexible and High-Reliable HW/SW Co-Design Method for Real-Time Embedded System" by T. KITANI, et al., pgs. 1-10.
	AW	"HY-C LRM 1.2 Rev 1.1" Y Explorations, Inc., Nov. 7, 2004.
	AX	
	AY	